ABSTRACT

There is provided a block matching processor and method for flexibly supporting block matching motion estimation at motion vector prediction modes using matching blocks of various sizes. Each of difference unit (D-unit) arrays takes each smallest size matching block, calculates the difference between the pixels of a current frame and the pixels of a reference frame, and converts the differences to absolute values. An accumulator generates SADs (Sum of Absolute Difference) for the smallest size matching blocks and SADs for all the matching blocks of various sizes by tree-like hierarchical addition of the absolute values of the smallest size matching blocks received from the D-unit arrays.